L Number	Hits	Search Text	DB	Time stamp
1	108777	capacitance$1	USPAT; US-PGPUB	2001/11/30 15:19
4	2203	connector$ same capacitance$1	USPAT; US-PGPUB	2001/11/30 15:20
7	66821	(elongated adj2 conductor$1) or ((metal or transmission) adj3 (trace$1 or line$1))	USPAT; US-PGPUB	2001/11/30 15:24
10	168	(connector$ same capacitance$1) same ((elongated adj2 conductor$1) or ((metal or transmission) adj3 (trace$1 or line$1)))	USPAT; US-PGPUB	2001/11/30 15:47
13	58735	439/$.ccls.	USPAT; US-PGPUB	2001/11/30 15:48
16	42	((connector$ same capacitance$1) same ((elongated adj2 conductor$1) or ((metal or transmission) adj3 (trace$1 or line$1)))) and 439/$.ccls.	USPAT; US-PGPUB	2001/11/30 15:48

US-CL-CURRENT: 326/30,326/86 ,326/93

US-PAT-NO: 6266730
DOCUMENT-IDENTIFIER: US 6266730 B1
TITLE: High-frequency bus system
DATE-ISSUED: July 24, 2001
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Perino; Donald V.	Los Altos	CA	N/A	N/A
Garrett, Jr.; Billy	Mountain View	CA	N/A	N/A
Wayne	Sunnyvale	CA	N/A	N/A
Liaw; Haw-Jyh	San Jose	CA	N/A	N/A
Nguyen; David	Santa Clara	CA	N/A	N/A
Nimmagadda; Srinivas	Mountain View	CA	N/A	N/A
Gasbarro; James A.	San Jose	CA	N/A	N/A
Crisp; Richard DeWitt				

US-CL-CURRENT: 710/300,326/30 ,326/86 ,326/93
ABSTRACT:
A high frequency bus system which insures uniform arrival times of high-fidelity signals to the devices on the high frequency bus, despite the use of the bus on modules and connectors. A high frequency bus system includes a first bus segment having one or more devices connected between a first and a second end. The first bus segment has at least a pair of transmission lines for propagating high frequency signals and the devices are coupled to the pair of transmission lines. The high frequency bus system also includes a second bus segment which has no devices connected to it. The second bus segment also has at least a pair of transmission lines for propagating high frequency signals. The first end of the first segment and second end of the second segment are coupled in series to form a chain of segments and when two signals are introduced to the first end of the second bus segment at the substantially the same time, they arrive at each device connected to the first bus segment at substantially the same time. Also, when two signals originate at a device connected to the first bus segment at substantially the same time, they arrive at the first end of the second bus segment at substantially the same time. Uniform arrival times hold despite the use of connectors to couple the segments together, despite the segments being located on modules, without the need for stubs, despite the presence of routing turns in the segments and despite the type of information, such as address, data or control, carried by the signals.
20 Claims, 26 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 21

DEPR:
When **connectors** are used as the means of coupling between bus segments, certain characteristics of the **connector** are important with respect to their effect on the **transmission lines** coupled by the **connector**. FIG. 12 shows a circuit model of a **connector and the transmission lines** on either side and near the connection made by the **connector**. Section 1240 shows an equivalent circuit representation of the **transmission line** segment on the motherboard near the **connector**. Section 1250 shows the segment of **transmission line** on the module near the **connector** and section 1260 shows a circuit model of the **connector**

itself. In the motherboard section 1240, the unloaded impedance of the line 1200 is Z0, which is preferably in the range of 22 to 32 ohms and more preferably 28 ohms. Motherboard section 1240 also shows the **capacitance** CMB by
capacitor 1220. This **capacitance** results from a through-hole, surface mount pad or other capacitive structure, placed on the mother board in the path of the line 1270. The **connector** section 1260 includes the **capacitance** CPIN of the
connector pin shown as capacitor 1240 and the inductance LPIN of the pin shown as inductor 1230. Finally, section 1250 includes a pad on the module having **capacitance** CPAD and shown as capacitor 1255. Line 1210 in module section 1250
has the same preferred impedance Z0 as the line 1200 in motherboard module 1240. By controlling the value of CMB and CPAD, the equivalent impedance of the pin is altered to become the preferred impedance Z0. It is preferred for **connectors** used in connection with an embodiment of the present invention that the pin inductance be in the range of 2 to 3 nanohenrys (Nh). A typical value is approximately 2.3 Nh. The pin **capacitance** is in the range of 0.5 to 1.0 pico-farads (Pf) and is typically about 0.6 Pf. If the value of CMB and CPAD are made to be about 1 Pf, the total **capacitance** near the **connector** is about 2.6 Pf and the total inductance is about 2.3 nH. The result is an effective impedance of about 28-30 ohms for the **connector**. Thus, a signal propagating from the motherboard section 1240 through the **connector** section 1260 on onto the module section 1250 encounters no significant change of impedance and no significant reflection is generated. Furthermore, the time to pass through the
connector, i.e., from beginning of section 1240 to the end of section 1250 is uniform across all of the signals.

DEPR:
FIG. 13A shows a circuit model for the **transmission line** segment on a module in
an embodiment of the present invention, where the term "module" implies the presence of devices connected to the **transmission line** segment. In this figure, connection points 1350 represent the coupling between the motherboard and the module, which may be by means of a **connector** whose characteristics were
discussed above. Line sections 1360 are those portions of the **transmission line** having impedance Z0 and no device connections, and line sections 1320 comprise sections of **transmission line** 1355 having an unloaded line impedance of Z1 and a device load 1340. FIG. 13B shows an equivalent circuit for the device load indicating that it can be modeled approximately as a capacitor CDL.
The value of CDL is approximately in the range of 2-3 Pf, but preferably about 2.5 Pf for a single device connection. To avoid discontinuities between the Z0
section of line 1360 and the portion of line 1320 having the device load, the Z1 impedance of line sections 1355 is increased substantially over the Z0 value
so that the equivalent impedance of line section 1320 matches that of the Z0 section 1360. If the nominal impedance of the Z0 section 1360 is about 28 ohms
and a device load is to a first order capacitive and approximately 2.5 pF, then
Z1 is made approximately 70 ohms. The result is that the additional **capacitance** reduces the impedance of section 1320 to about 28 ohms according to
the well known relationship that the loaded impedance Z1' equals the unloaded

impedance Z1 multiplied by the square root of the ratio of the unloaded **capacitance** C1 to the total **capacitance** CT.

US-CL-CURRENT: 439/955

US-PAT-NO: 6244907
DOCUMENT-IDENTIFIER: US 6244907 B1
TITLE: Selectable compatibility electrical connector assembly
DATE-ISSUED: June 12, 2001
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Arnett; Jaime Ray	Fishers	IN	N/A	N/A

US-CL-CURRENT: 439/676,439/955

ABSTRACT:
A selectable compatibility electrical connector assembly has a high performance plug for mating with the jack to form a high performance electrical connection or to provide switching among various circuit elements to change the transmission characteristics of the assembly. The jack is adapted to receive low performance plugs and has a plug stop therein for limiting the depth of insertion of the low performance plug into the jack. The plug of the invention has an elongated notch in its front end which is designed to clear the plug stop for insertion of the plug to a depth greater than that of the low performance plug. The jack has first and second longitudinally offset latching stubs for latching both the low performance and the high performance plug at their proper insertion depth. An embodiment of the jack has a reciprocating switch assembly adapted to be actuated by the high performance plug when inserted to its proper depth in the jack.
23 Claims, 17 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 7

BSPR:
Telecommunication equipment has benefited from the design of electrical plugs and jacks that provide easy connect/disconnect capability between electrical circuits within the telecommunications equipment and, for example, local network wiring. Such plugs and jacks are particularly popular in association with telephone sets, where they were first used, and, more recently, in association with a large variety of peripheral equipment that is connected to telephone lines. The modular plugs and jacks in use today have been standardized insofar as their performance specifications are concerned and also insofar as certain critical dimensions and structural features are concerned. The use of these devices has become so widespread that new houses and other buildings are prewired with jacks located throughout the various rooms as well as other strategic locations, to accommodate the communication equipment. Where large numbers of such connections are needed, it is typical practice to route the wires to a central location, such as a communication closet where, typically, the jacks are mounted on patch panels. Such an arrangement is shown, for example, in U.S. Pat. No. 5,096,439 of J. R. Arnett. In most installations, it is desirable that the jack be compact, and there have been numerous jacks designed to achieve this goal. In U.S. Pat. No. 5,096,442 of J. R. Arnett there is shown one such compact jack and plug arrangement which, together, constitute a compact electrical **connector**. The compact electrical **connector** shown in that patent includes a metallic lead frame mounted to a spring block. The lead frames comprise a number of flat **elongated conductors,**

each terminating in a spring contact at one end and an insulation displacement **connector** at the other end. The insulation displacement **connectors** are folded around opposite side walls of the spring block and achieve compactness, and the spring contacts are folded around the front surface of the spring block for insertion into a jack frame. The front surface of the spring block includes a tongue-like projection which fits into one end of the jack frame and interlocks therewith. With the ever increasing numbers of peripheral equipment, and with concomitant increases in operating frequencies, such as required in digital data transmission, **connector** assemblies such as shown in the aforementioned Arnett '442 patent, while enjoying a large amount of commercial success, do not function well in the higher frequency ranges. The use of such plugs and jacks is impaired by crosstalk within the components, especially in the plug, and as frequencies increase, so does the effect of crosstalk. Numerous arrangements have been proposed for reducing the effects of crosstalk overall by **connectors** having a minimum of crosstalk, or by **connectors** which add compensating crosstalk to the overall circuit, such as adding **capacitance** to the jack to nullify or compensate for the crosstalk in the plug. In U.S. Pat. No. 5,186,647 of W. J. Denkmann et al., there is shown an electrical **connector** for conducting high frequency signals in which the input and output terminals are interconnected by a pair of metallic lead frames mounted on a dielectric spring block. The lead frames, which are substantially identical to each other each comprises several flat **elongated conductors,** terminating in spring contacts at one end and insulation displacement **connectors** at the other end. The conductors are generally parallel and close to each other, but three conductors of one frame are arranged to overlap three conductors of the other frame in a crossover region. As a result, the crosstalk between the several conductors is reduced, due to the reversal in polarities caused by the crossovers.

US-CL-CURRENT: 200/51.06,439/941

US-PAT-NO: 6168472
DOCUMENT-IDENTIFIER: US 6168472 B1
TITLE: Selectable compatibility electrical connector assembly
DATE-ISSUED: January 2, 2001
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Arnett; Jaime Ray	Fishers	IN	N/A	N/A

US-CL-CURRENT: 439/676,200/51.06 ,439/941

ABSTRACT:
A selectable compatibility electrical connector assembly has a high performance jack and a high performance plug for mating with the jack to form a high performance electrical connection. The jack is adapted to receive low performance plugs and has a movable member therein for altering the transmission loss characteristic of the connector by introducing or removing circuit elements into or from the connector circuit depending upon whether a low performance plug or the high performance plug is inserted in the jack. The plug is adapted to be inserted into a low performance jack and has a movable member therein for altering the transmission loss characteristic of the connector by introducing or removing circuit elements into or from the connector circuit depending upon whether the plug is inserted into or removed from a low performance jack.
11 Claims, 11 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 8

BSPR:
Telecommunication equipment has benefited from the design of electrical plugs and jacks that provide easy connect/disconnect capability between electrical circuits within the telecommunications equipment and, for example, local network wiring. Such plugs and jacks are particularly popular in association with telephone sets, where they were first used, and, more recently, in association with a large variety of peripheral equipment that is connected to telephone lines. The modular plugs and jacks in use today have been standardized, insofar as their performance specifications are concerned and also insofar as certain critical dimensions and structural features are concerned. The use of these devices has become so widespread that new houses and other buildings are prewired with jacks located throughout the various rooms as well as other strategic locations, to accommodate the communication equipment. Where large numbers of such connections are needed, it is typical practice to route the wires to a central location, such as a communication closet where, typically, the jacks are mounted on patch panels. Such an arrangement is shown, for example, in U.S. Pat. No. 5,096,439 of J. R. Arnett. In most installations, it is desirable that the jack be compact, and there have been numerous jacks designed to achieve this goal. In U.S. Pat. No. 5,096,442 of J. R. Arnett there is shown one such compact jack and plug arrangement. The compact electrical **connector** shown in that patent includes a metallic lead frame mounted to a spring block. The lead frames comprise a number of flat **elongated conductors,** each terminating in a spring contact at one end and an insulation displacement **connector** at the other end. The insulation displacement **connectors** are folded around opposite side walls of the spring block and achieve compactness, and the spring contacts are folded

around
the front surface of the spring block for insertion into a jack frame. The front surface of the spring block includes a tongue-like projection which fits into one end of the jack frame and interlocks therewith. With the ever increasing numbers of peripheral equipment, and with concomitant increases in operating frequencies, such as required in digital data transmission, **connector**
assemblies such as shown in the aforementioned Arnett '442 patent, while enjoying a large amount of commercial success, do not function well in the higher frequency ranges. The use of such plugs and jacks is impaired by crosstalk within the components, especially in the plug, and as frequencies increase, so does the effect of crosstalk. Numerous arrangements have been proposed for reducing the effects of crosstalk overall by **connectors** having a minimum of crosstalk, or by **connectors** which add compensating crosstalk to the overall circuit, such as adding **capacitance** to the jack to nullify or compensate for the crosstalk in the plug. In U.S. Pat. No. 5,186,647 of W. J. Denkmann et al., there is shown an electrical **connector** for conducting high frequency signals in which the input and output terminals are interconnected by
a pair of metallic lead frames mounted on a dielectric spring block. The lead frames, which are substantially identical to each other each comprises several flat **elongated conductors,** terminating in spring contacts at one end and insulation displacement **connectors** at the other end. The conductors are generally parallel and close to each other, but three conductors of one frame are arranged to overlap three conductors of the other frame in a crossover region. As a result, the crosstalk between the several conductors is reduced, due to the reversal in polarities caused by the crossovers.

US-CL-CURRENT: 365/191

US-PAT-NO: 6166971
DOCUMENT-IDENTIFIER: US 6166971 A
TITLE: Method of and apparatus for correctly transmitting signals at high speed without waveform distortion
DATE-ISSUED: December 26, 2000
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Tamura; Hirotaka	Kawasaki	N/A	N/A	JPX
Takauchi; Hideki	Kawasaki	N/A	N/A	JPX
Cheung; Tsz-shing	Kawasaki	N/A	N/A	JPX
Gotoh; Kohtaroh	Kawasaki	N/A	N/A	JPX

US-CL-CURRENT: 365/198,365/191
ABSTRACT:
A driver circuit transmits a signal to a receiver circuit through a signal transmission line. The driver circuit has an output driver, a front driver, and a level adjuster. The front driver drives the output driver, and the level
adjuster adjusts the output level of the front driver. The output driver generates a signal whose level is variable in response to an output level of the front driver.
24 Claims, 91 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 77

DEPR:
FIG. 61 shows a signal transmission system according to a prior art. This system is applicable to signal transmission between, for example LcIs. The system involves a driver circuit 4101, a signal **transmission line** (cable) 4102,
parasitic inductance elements 4131 to 4133, parasitic **capacitance** elements 4141
to 4145, a terminating resistor 4105, and a receiver circuit 4106. The parasitic inductance element 4131 may be of bonding wires for connecting a semiconductor chip (driver circuit) to external pins, the parasitic inductance element 4132 of a package and lead wires, and the parasitic inductance element 4133 of **connectors**. The parasitic **capacitance** elements 4141 to 4145 correspond
to parasitic capacitors formed at respective parts.

US-CL-CURRENT: 439/941

US-PAT-NO: 6165023
DOCUMENT-IDENTIFIER: US 6165023 A
TITLE: Capacitive crosstalk compensation arrangement for a communication connector
DATE-ISSUED: December 26, 2000
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Troutman; Dennis Lamar	Fishers	IN	N/A	N/A
Spitz; William Tracy	Indianapolis	IN	N/A	N/A

US-CL-CURRENT: 439/676,439/941
ABSTRACT:

A communication connector arrangement has a contact wire support, and at least a first and a second pair of terminal contact wires with portions fixed on the support. Each pair of contact wires has contact portions for establishing electrical connections with a mating connector. A first leading portion of a first contact wire of the first pair, and a second leading portion of a second contact wire of the second pair, extend generally parallel to one another and are terminated at their ends by a capacitance element. Capacitive crosstalk compensation is thus produced at the contact portions of the terminal contact wires, when the latter are engaged by the mating connector. In a disclosed embodiment, the arrangement includes a jack frame joined with the contact wire support, and the terminal contact wires are positioned inside a connector opening in the jack frame to connect electrically with a plug connector when inserted in the connector opening in the frame.
12 Claims, 6 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 5

DEPR:
A determined compensation **capacitance** element 64 is connected between the terminals 62d and 62f in the base support 52. Further, a determined compensation **capacitance** element 66 is connected between the terminals 62c, 62e, in the base support 52. Capacitive crosstalk compensation is thus conveyed to the zone of contact 58 from the **capacitance** elements 64, 66, via the leading portions 60d and 60f; and 60c and 60e, for the associated terminal contact wires of pairs 1 and 3. The parallel leading portions 60d and 60f; and 60c and 60e, thus may be viewed as open-circuited **transmission lines** having electrically short lengths and acting to produce capacitive compensation coupling in an amount determined by the **capacitance** elements 64, 66, in the base support 12. An important feature of the **connector** assembly 50, therefore, is that it allows flexibility for adjusting the value of capacitive crosstalk compensation introduced at the zone of contact 58, for example, by merely altering circuit board artwork in the base support 52 which artwork determines the values of each of the **capacitance** elements 64, 66.

US-CL-CURRENT: 439/941

US-PAT-NO: 6139371
DOCUMENT-IDENTIFIER: US 6139371 A
TITLE: Communication connector assembly with capacitive crosstalk compensation
DATE-ISSUED: October 31, 2000
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Troutman; Dennis Lamar	Fishers	IN	N/A	N/A
Spitz; William Tracy	Indianapolis	IN	N/A	N/A

US-CL-CURRENT: 439/676,439/941
ABSTRACT:

A communication connector assembly has a base support, and at least first and second pairs of terminal contact wires with base portions mounted on the base support. The free end portions of the contact wires define a zone of contact within which electrical connections are established with a mating connector, and each pair of contact wires defines a different signal path in the connector assembly. The first and the second pair of contact wires have corresponding leading portions extending from the free end portions, to a side of the zone of contact opposite from the base portions. A leading portion of a
contact wire of the first pair, and a leading portion of a contact wire of the second pair, are constructed and arranged for capacitively coupling to one another thus conveying capacitive crosstalk compensation to the zone of contact
where offending crosstalk is introduced by a mated connector.
12 Claims, 6 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 5

DEPR:
A determined compensation **capacitance** element 64 is connected between the terminals 62d and 62f in the base support 52. Further, a determined compensation **capacitance** element 66 is connected between the terminals 62c, 62e, in the base support 52. Capacitive crosstalk compensation is thus conveyed to the zone of contact 58 from the **capacitance** elements 64, 66, via the leading portions 60d, and 60f; and 60c, and 60e, for the associated terminal contact wires of pairs 1 and 3. The parallel leading portions 60d, and 60f; and 60c, and 60e, thus may be viewed as open-circuited **transmission lines** having electrically short lengths and acting to produce capacitive compensation coupling in an amount determined by the **capacitance** elements 64, 66, in the base support 12. An important feature of the **connector** assembly 50,
therefore, is that it allows flexibility for adjusting the value of capacitive crosstalk compensation introduced at the zone of contact 58, for example, by merely altering circuit board artwork in the base support 52 which artwork determines the values of the elements 64, 66.

US-CL-CURRENT: 200/51.06,439/170 ,439/955

US-PAT-NO: 6139343
DOCUMENT-IDENTIFIER: US 6139343 A
TITLE: Selectable compatibility electrical connector plug
DATE-ISSUED: October 31, 2000
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Arnett; Jaime Ray	Fishers	IN	N/A	N/A

US-CL-CURRENT: 439/188,200/51.06 ,439/170 ,439/955
ABSTRACT:

A selectable compatibility plug has a substantially hollow housing member and a plurality of contact members extending from a cable connection end to a connector end. A movable circuit member is contained in the housing for translational movement, the circuit members having circuit components on a surface thereof that is in contact with the contact members. Actuator means for moving the circuit member from a first position to a second position is mounted to the circuit member and adapted to be actuated when the plug is inserted in a low performance jack to cause the contact members to contact certain ones of the circuit elements.

18 Claims, 11 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 8

BSPR:

Telecommunication equipment has benefited from the design of electrical plugs and jacks that provide easy connect/disconnect capability between electrical circuits within the telecommunications equipment and, for example, local network wiring. Such plugs and jacks are particularly popular in association with telephone sets, where they were first used, and, more recently, in association with a large variety of peripheral equipment that is connected to telephone lines. The modular plugs and jacks in use today have been standardized, insofar as their performance specifications are concerned and also insofar as certain critical dimensions and structural features are concerned. The use of these devices has become so widespread that new houses and other buildings are prewired with jacks located throughout the various rooms as well as other strategic locations, to accommodate the communication equipment. Where large numbers of such connections are needed, it is typical practice to route the wires to a central location, such as a communication closet where, typically, the jacks are mounted on patch panels. Such an arrangement is shown, for example, in U.S. Pat. No. 5,096,439 of J. R. Arnett. In most installations, it is desirable that the jack be compact, and there have been numerous jacks designed to achieve this goal. In U.S. Pat. No. 5,096,442 of J. R. Arnett there is shown one such compact jack and plug arrangement. The compact electrical **connector** shown in that patent includes a metallic lead frame mounted to a spring block. The lead frames comprise a number of flat **elongated conductors,** each terminating in a spring contact at one end and an insulation displacement **connector** at the other end. The insulation displacement **connectors** are folded around opposite side walls of the
spring block and achieve compactness, and the spring contacts are folded around
the front surface of the spring block for insertion into a jack frame. The front surface of the spring block includes a tongue-like projection which fits into one end of the jack frame and interlocks therewith. With the ever increasing numbers of peripheral equipment, and with concomitant increases in

operating frequencies, such as required in digital data transmission, **connector**
assemblies such as shown in the aforementioned Arnett '442 patent, while enjoying a large amount of commercial success, do not function well in the higher frequency ranges. The use of such plugs and jacks is impaired by crosstalk within the components, especially in the plug, and as frequencies increase, so does the effect of crosstalk. Numerous arrangements have been proposed for reducing the effects of crosstalk overall by **connectors** having a minimum of crosstalk, or by **connectors** which add compensating crosstalk to the overall circuit, such as adding **capacitance** to the jack to nullify or compensate for the crosstalk in the plug. In U.S. Pat. No. 5,186,647 of W. J. Denkmann et al., there is shown an electrical **connector** for conducting high frequency signals in which the input and output terminals are interconnected by
a pair of metallic lead frames mounted on a dielectric spring block. The lead frames, which are substantially identical to each other each comprises several flat **elongated conductors,** terminating in spring contacts at one end and insulation displacement **connectors** at the other end. The conductors are generally parallel and close to each other, but three conductors of one frame are arranged to overlap three conductors of the other frame in a crossover region. As a result, the crosstalk between the several conductors is reduced, due to the reversal in polarities caused by the crossovers.

US-CL-CURRENT: 439/941

US-PAT-NO: 6089923
DOCUMENT-IDENTIFIER: US 6089923 A
TITLE: Jack including crosstalk compensation for printed circuit board
DATE-ISSUED: July 18, 2000
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Phommachanh; Chansy	Shakopee	MN	N/A	N/A

US-CL-CURRENT: 439/676,439/941
ABSTRACT:

A forward-reverse crosstalk compensation method is provided for compensating capacitance/inductance on a printed circuit board of a connector. The method includes a forward compensation process and a reverse compensation process. The forward compensation process compensates the unbalanced capacitance in the plug of the connector by using the parallel conductive lines or wires. The reverse compensation process can be used to compensate the unbalance capacitance/inductance caused by the forward compensations in the same pair combination of the connector. In both forward compensation and reverse compensation processes, electro-magnetic fields, such as capacitors, can be formed to balance the capacitance/inductance on the printed circuit board of the connector.

14 Claims, 19 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 7

BSPR:

In one aspect of the present invention, the method of compensating crosstalk in a **connector** arrangement includes: providing a plurality of pairs of conductors on a printed circuit board, the pairs of conductors connecting to respective front and rear terminals, each pair of conductors including a ring conductor and a tip conductor, and the ring and tip conductors being substantially disposed in parallel to control the **transmission line** impedence; sending electrical signals between the front and rear terminals; generating forward-compensating **capacitance,** induced between two of the pairs of conductors, proximate the respective front terminals by providing a first capacitor between a first conductor of the first pair and a second conductor of the second pair and providing a second capacitor between a second conductor of the first pair and a first conductor of the second pair; and generating reverse-compensating capacitance/inductance to compensate the unbalanced capacitance/inductance induced between the two pairs of conductors by the first and second capacitors at the front terminal. The reverse-compensating capacitance/inductance is disposed proximate the rear terminals by providing a third capacitor between the first conductor of the first pair and the first conductor of the second pair and providing a fourth capacitor between the second conductor of the first pair and the second conductor of the second pair.

US-CL-CURRENT: 174/117F,174/117FF ,174/158R ,174/261 ,174/268 ,174/32 ,333/238 ,361/679 ,361/686 ,361/777 ,361/803 ,**439/59** ,**439/61**

US-PAT-NO: 5930119
DOCUMENT-IDENTIFIER: US 5930119 A
TITLE: Backplane having reduced LC product
DATE-ISSUED: July 27, 1999
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Berding; Andrew R.	Scottsdale	AZ	N/A	N/A

US-CL-CURRENT: 361/788,174/117F ,174/117FF ,174/158R ,174/261 ,174/268 ,174/32 ,333/238 ,361/679 ,361/686 ,361/777 ,361/803 ,**439/59** ,**439/61**

ABSTRACT:
A data processing system includes a backplane and a plurality of logic boards connected to the backplane by a plurality of connectors. A set of common points is electrically coupled to the connectors by individual conductive traces between each common point and the corresponding pins of the connectors. The inductance of longer traces is reduced by merging traces near a central portion of the backplane to form a conductive region that extends to at least one connector on either side of the common points, thereby electrically shortening the longer traces. The inductance is further reduced by widening the longer traces. Longer traces are wider than shorter traces to reduce the differences in the LC products associated with each trace and, therefore, the differences in delay among the traces.
13 Claims, 5 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 2

DEPR:
Connecting the pins by individual traces that join at a common point causes the
circuit to act like a simple lumped inductance and **capacitance** rather than as a
complex **transmission line**. The **capacitances** of the traces, of the **connectors**, of the stubs into the boards, and of the semiconductor devices on the boards act as if they were lumped at the common point rather than being distributed along a trace. The lumped **capacitance** is driven through the lumped inductance of the trace from a driver board. The effective circuit is a series connected inductor and a shunt capacitor to ground at the common point.

CCXR:
439/59

CCXR:
439/61

L Number	Hits	Search Text	DB	Time stamp
-	17	bitstream adj storage	USPAT	2000/10/17 14:51
-	363	source adj synchronous	USPAT; US-PGPUB	2001/11/30 10:02
-	12162	710/$.ccls.	USPAT; US-PGPUB	2001/11/30 10:03
-	10533	326/$.ccls.	USPAT; US-PGPUB	2001/11/30 10:03
-	1	(source adj synchronous) and 710/$.ccls. and 326/$.ccls.	USPAT; US-PGPUB	2001/11/30 11:01
-	83083	clock$3 adj2 signal$1	USPAT; US-PGPUB	2001/11/30 11:00
-	3033	"250" adj mhz	USPAT; US-PGPUB	2001/11/30 11:01
-	76	(clock$3 adj2 signal$1) same ("250" adj mhz)	USPAT; US-PGPUB	2001/11/30 11:02
-	0	((clock$3 adj2 signal$1) same ("250" adj mhz)) and 710/$.ccls. and 326/$.ccls.	USPAT; US-PGPUB	2001/11/30 11:02
-	5	((clock$3 adj2 signal$1) same ("250" adj mhz)) and 710/$.ccls.	USPAT; US-PGPUB	2001/11/30 11:03
-	724	rambus	USPAT; US-PGPUB	2001/11/30 11:03
-	1	((clock$3 adj2 signal$1) same ("250" adj mhz)) same rambus	USPAT; US-PGPUB	2001/11/30 11:05
-	9327	"300" adj mhz	USPAT; US-PGPUB	2001/11/30 11:05
-	1708	"800" adj mhz	USPAT; US-PGPUB	2001/11/30 11:05
-	0	rambus same (("300" adj mhz) same ("800" adj mhz))	USPAT; US-PGPUB	2001/11/30 11:06
-	0	rambus and (("300" adj mhz) same ("800" adj mhz))	USPAT; US-PGPUB	2001/11/30 11:06
-	32	("300" adj mhz) same ("800" adj mhz)	USPAT; US-PGPUB	2001/11/30 11:06
-	0	(clock$3 adj2 signal$1) same (("300" adj mhz) same ("800" adj mhz))	USPAT; US-PGPUB	2001/11/30 11:07
-	2	(clock$3 adj2 signal$1) and (("300" adj mhz) same ("800" adj mhz))	USPAT; US-PGPUB	2001/11/30 11:14
-	0	(source adj synchronous) and (("300" adj mhz) same ("800" adj mhz))	USPAT; US-PGPUB	2001/11/30 11:14
-	0	710/$.ccls. and (("300" adj mhz) same ("800" adj mhz))	USPAT; US-PGPUB	2001/11/30 11:15
-	0	326/$.ccls. and (("300" adj mhz) same ("800" adj mhz))	USPAT; US-PGPUB	2001/11/30 11:15

US-CL-CURRENT: 326/121,326/21 ,326/30 ,326/80 ,326/81 ,326/83 ,326/86 ,327/309 ,710/100 ,710/107

US-PAT-NO: 6272577
DOCUMENT-IDENTIFIER: US 6272577 B1
TITLE: Data processing system with master and slave devices and asymmetric signal swing bus
DATE-ISSUED: August 7, 2001
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
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US-CL-CURRENT: 710/110,326/121 ,326/21 ,326/30 ,326/80 ,326/81 ,326/83 ,326/86 ,327/309 ,710/100 ,710/107

ABSTRACT:
A memory device which utilizes a plurality of memory modules coupled in parallel to a master I/O module through a single directional asymmetrical signal swing (DASS) bus. This structure provides an I/O scheme having symmetrical swing around half the supply voltage, high through-put, high data bandwidth, short access time, low latency and high noise immunity. The device utilizes improved column access circuitry including an improved address sequencing circuit and a data amplifier within each memory module. A resynchronization circuit allows the device to operate either synchronously and asynchronously using the same pins. Each memory module has independent address and command decoders to enable independent operation so that each memory module is activated by commands on the DASS bus only when a memory access operation is performed within the particular memory module. Redundant memory modules are included to replace defective memory modules, and replacement can be carried out through commands on the DASS bus. The memory device can be configured to simultaneously write a single input data stream to multiple memory modules or to perform high-speed interleaved read and write operations. In one embodiment, multiple memory devices are coupled to a common, high-speed I/O bus without requiring large bus drivers and complex bus receivers in the memory modules.
49 Claims, 27 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 24

BSPR:
Memory devices in accordance with the present invention can be accessed both synchronously and asynchronously using the same set of connection pins. This is achieved using the following techniques: (i) using a self-timed control in connection with the previously described circuit-module architecture. (ii) connecting memory modules in parallel to an on-chip bus which uses **source synchronous** clocking. (iii) using half clock-cycle (single clock-transition) command protocol. (iv) using an on-chip resynchronization technique. This results in memory devices that have short access latency (about 10 ns), and high data bandwidth (1 gigabyte/sec).

DEPR:
On DASS bus 102, **source synchronous** transfer is used to meet the synchronous and asynchronous operation requirements. A source clock (Sck) signal and a destination clock (Dck) signal on DASS bus 102 facilitate the **source synchronous** timing. The Sck signal is used to synchronize data, addresses and commands from the master I/O module 104 to memory modules 111-128. The Dck signal is generated by one of the memory modules 111-128 selected for access to
provide synchronization timing for data transmitted from memory modules 111-128
to I/O module 104.

CCOR:
710/110

CCXR:
326/121

CCXR:
326/21

CCXR:
326/30

CCXR:
326/80

CCXR:
326/81

CCXR:
326/83

CCXR:
326/86

CCXR:
710/100

CCXR:
710/107

US-CL-CURRENT: 365/230.01,365/230.05 ,711/105 ,711/154

US-PAT-NO: 6230245
DOCUMENT-IDENTIFIER: US 6230245 B1
TITLE: Method and apparatus for generating a variable sequence of memory device command signals
DATE-ISSUED: May 8, 2001
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Manning; Troy A.	Boise	ID	N/A	N/A

US-CL-CURRENT: 711/167,365/230.01 ,365/230.05 ,711/105 ,711/154

ABSTRACT:
A command generator for a dynamic random access memory decrements a counter from an initial counter value which is a function of the clock speed. The output of the counter is decoded to generate various command signals for the DRAM. In particular, each command signal is generated by a respective counter value, with the correspondency between counter values and command signals being
a function of the clock speed. The counter decrements from larger initial values at higher clock speeds, and the command signals are generally issued by the decoder at higher counter values for higher clock speeds. As a result of the lack of correspondency between the timing of the command signals and the number of clock cycles occurring during a memory access, the timing of the command signals may be selected to optimize the speed of the DRAM desired despite substantial variations in clock speed.
60 Claims, 12 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 11

BSPR:
In the operation of a dynamic random access memories ("DRAMs"), specific functions must occur in a predetermined sequence. These functions are generally performed responsive to respective command signals issued by a command generator. The timing of the command signals is generally controlled by a **clock signal** either registered to an edge of the **clock signal** or occurring
a predetermined time after an edge of the **clock signal**. The rate at which the DRAM may process commands is limited by the amount of time it takes to perform functions responsive to the commands. For most functions, the minimum times to
perform the functions are specified by the manufacturer of the DRAM. however, since the commands are generally issued responsive to **clock signals,** the amount
of time that the DRAM has to perform its functions is controlled by the clock speed. For example, as illustrated in FIG. 1A, a memory read command 10 is issued by a conventional memory controller and is registered with a **clock signal** 12 at time t.sub.0. As further shown in FIG. 1A, it requires four clock
cycles to complete the read operation because of the many operations that must occur in a DRAM before data can be read from the DRAM. Thus, a data bit 14 is not present on the data bus until time t.sub.1. The elapsed time from issuing the read command 10 to the complete processing of the command by applying the data bit 14 to the data bus is therefore .DELTA.t.sub.a. The elapsed time could be reduced by increasing the speed of the clock 12. However, regardless of the speed of the clock, the DRAM requires a certain minimum time to complete

its functions. Speeding the clock up beyond that point will not reduce the amount of time required to perform those functions.

BSPR:
Although DRAMs are operating at optimum speed when the clock is at or near its maximum speed, they operate a far from optimum speed responsive to slower clock
speeds. With reference to FIG. 1B, a **clock signal** 20 has a speed or frequency only half that of the clock 12 in FIG. 1A. Once again, a read command 22 is registered with the clock 20 at time t.sub.0, and a data bit 24 is applied to the data bus four clock cycles later. However, because of the slower speed clock 20, the data bit 24 is not applied to the data bus until t.sub.2. As a result of the slower clock speed, the elapsed time between issuing of the read command 22 and complete processing of the command is .DELTA.t.sub.b which is twice the duration of .DELTA.t.sub.a. Thus, by employing a fixed relationship between a **clock signal** and the issuing of command signals, conventional DRAMs often operate at far from optimum speed when they receive a relatively slow **clock signal**.

BSPR:
It will be understood by one skilled in the art that the timing diagrams of FIGS. 1A and 1B omit a large number of other signals applied to the DRAM. These signals have been omitted for purposes of brevity. Also, one skilled in the art will understand that the command signals 10, 22 are, in reality, composed of a combination of other signals which are commonly referred to as simply a command. The exact nature of these signals will depend on the nature of the DRAM, but the principle explained above is applicable to all type of DRAMs, including asynchronous DRAMs, synchronous DRAMs, and packetized DRAMs. Also, although the problem resulting from issuing command signals according to a fixed relationship with the **clock signal** has been explained with reference to
DRAMs, the explanation of the problem as well as the solution provided by the preferred embodiment of the invention are applicable to other integrated circuits that issue command signals or the like responsive to a **clock signal**.

BSPR:
A command generator for generating command signals for a memory device includes
a sequencer generating a sequence of command signals responsive to a **clock signal** that may have one of a plurality of clock speeds. Each of the sequences
of command signals preferably corresponds to a respective clock speed, and the sequencer selects one of the sequences as a function of the clock speed. The sequencer may include a counter and a decoder. The counter receives the **clock signal** and provides a counter value that increments or decrements responsive to
the **clock signal**. The decoder generates one of a plurality of sequences of command signals, with the command signals in each sequence corresponding to respective counter values. Each of the sequences of command signals corresponds to a respective clock speed, and the decoder selects one of the sequences as a function of the clock speed. Thus, the correspondency between each command signal and its respective counter value is a function of the clock
speed. The command generator may also include a counter load circuit coupled to the counter. The counter load circuit loads an initial count into the counter that is a function of the clock speed. The counter then increments or decrements from the initial value responsive to the **clock signal**. The command generator may also include a counter enable circuit generating a counter enable

signal to permit the counter to increment or decrement responsive to the **clock signal**. The counter enable circuit MAY include a latch circuit and a counter start circuit. The latch circuit generates the counter enable signal responsive to a start signal and terminates the counter enable signal responsive to a stop signal. The counter start circuit generates the start signal and includes a clock detector detecting predetermined portions of the **clock signal**, and a variable delay enable circuit coupled to the clock detector. The variable delay enable circuit generates the start signal responsive to one of the detected predetermined portions of the **clock signal** after a predetermined number of cycles of the **clock signal** have elapsed from receiving a flag signal. The command generator may be used in any type of dynamic random access memory or other circuit which may be part of a computer system.

DRPR:
FIGS. 1A and 1B are timing diagrams illustrating the relationship between **clock signals** and the processing of commands in a conventional dynamic random access memory.

DEPR:
Before describing the preferred embodiment of the invention, the theory of operation of the preferred embodiment will be explained with reference to FIG. 2. FIG. 2 is a diagram representing the status of a counter and decoder (described below) in which the counter decrements responsive to a **clock signal** from an initial value to 0. The maximum initial value of the counter is 255. At various counter values, the decoder issues respective DRAM read command signals, some of which are shown in FIG. 2. Listed in the left-hand side of the diagram opposite their respective counter values are the command signals issued by the decoder when the frequency of the **clock signal** is 800 MHz. Listed in the right-hand side of the diagram in FIG. 2 opposite their respective counter values are those same command signals as they occur when the frequency of the **clock signal** is 400 MHz.

DEPR:
As further shown in FIG. 2, these same read commands are also issued by the decoder when the clock speed is 400 MHz, except that they are issued at substantially lower count values and the counter begins decrementing from about 150. The external row address is then latched at about count 135, the row address is decoded at about count 120, the row is precharged and equilibrated at about count 96, an externally applied column address is decoded at about count 70, the sense amps for the column address are enabled at about count 50, the addressed row is enabled at about count 32, and the data path couples data from the digit lines of the enabled sense amplifier to the external data bus terminal at about count 10. Note that, even though the command signals listed on the right-hand side of FIG. 2 are issued at substantially later count values, they occur at substantially the same time from the start of a memory access. Although approximately twice as many clock pulses may occur between the command signals when the clock frequency is 800 MHz as compared to 400 MHz, the command signals are nevertheless issued at the same times because of the higher clock speed. However, it should be emphasized that the timing of the command signals may not be entirely linear. For example, a command signal that may be issued at counter value 40 for a 400 MHz **clock signal** may not be issued at counter value 80 for an 800 MHz **clock signal**. However, a given command

signal will normally be issued at a higher counter value for a higher clock frequency. By eliminating a fixed relationship between the number of clock cycles and the issuing of command signals, the command generator is able to issue command signals at an optimum rate for a wide variety of clock speeds.

DEPR:
A block diagram of a preferred embodiment of a Command Generator 26 according to the invention is illustrated in FIG. 3. The operation of much of the Command Generator 26 illustrated in FIG. 3 is controlled by a **clock signal** CLK and a quadrature **clock signal** CLK 90 generated by a conventional clock circuit 28. A register 30 includes a plurality of storage cells corresponding in number to the number of possible different clock speeds. One of these plurality of clock speeds is designated by a SELECT signal. The SELECT signal may be generated by user action, by software, or by another circuit. Alternatively, a register designating the clock speed using other data formats,
such as binary, may be used. However, in the register 300 illustrated in FIG. 3, one and only one of the storage cells will contain a logic "1" to designate the corresponding clock speed as the speed of the **clock signals** output from the
clock circuit 28. The output of the register 30 is applied to a number of circuits, as explained in greater detail below.

DEPR:
A sequence of command signals is initiated by a positive going FLAG signal applied to a shift register 34 containing seven shift stages designated F.sub.0
-F.sub.6. The operation of the shift register 34 is best explained with reference to the timing diagram of FIG. 4. As shown in FIG. 4, the shift register 34 receives the **clock signal** CLK from the clock circuit 28 as well as a positive going FLAG signal at time t.sub.0. The FLAG signal is shifted into the first stage of the shift register 34 by the rising CLK edge at time t.sub.1, it is shifted into the second stage of the shift register 34 by the next CLK edge at time t.sub.2. Thereafter, the high FLAG signal is successively shifted through each of the remaining stages F.sub.1 -F.sub.6 by each CLK edge transition (both negative going and positive going). For example, the F.sub.2 pulse occurs at time t.sub.3, and the F.sub.4 pulse occurs
at time t.sub.5, etc. Thus, the delay from the receipt of the FLAG signal to shifting the FLAG signal into each shift stage F.sub.0 -F.sub.6 incrementally increases with each successive F value. As explained below, the pulses from the later shift stages, e.g., F.sub.6, are used to initiate a sequence of command signals at higher clock speeds while a pulse from a lower shift stage (e.g., F.sub.4) is used to initiate a sequence of command signals at lower clock speeds. However, since the clock speed is higher when the F.sub.6 pulse is used to initiate the sequence, the time between the FLAG signal and the F signal initiating the sequence of command signals varies to a lesser extent.

DEPR:
Returning, now, to FIG. 3, the F signal at the output of the shift register 34 is applied to a Counter Start Logic circuit 40 along with the SPEED signal indicative of the clock speed. As explained in detail below, the Counter Start
Logic circuit 40 generates a START signal responsive to the F signal registered
to either the rising or falling edge of the **clock signal** CLK. As mentioned above, the Counter Logic Circuit 40 uses a more delayed F signal for higher clock speeds. As a result, the Counter Start Logic circuit 40 generates the START signal after a variable number of clock cycles from the FLAG signal.

The
number of clock cycles is larger for higher clock speeds and lower for lower clock speeds.

DEPR:
As explained above with reference to FIG. 2, the Counter 50 is an 8 stage quadrature counter which decrements from 255 to 0 responsive to the **clock signals,** CLK and clock CLK 90. However, the Counter 50 may have a larger or smaller number of stages, and it may be other than a conventional counter using
quadrature **clock signals**. An initial counter value LD CNT is loaded into the Counter 50 from a Load Register 52 responsive to a LOAD signal which is applied
from other circuitry in the integrated circuit (not shown). The LD CNT value loaded into the Counter 50 is determined by the speed signal SPEED and a Device
Speed value applied from other circuitry in the integrated circuit (not shown).
Basically, the Load Register 52 stores respective initial counter values for the eight possible clock speeds designated by the register 30 and, for each of these eight possible clock speeds, a variety of initial counter values depending upon the maximum device operating speed. Thus, in the example explained above with reference to FIG. 2, the LD CNT value for an 800 MHz clock
speed is 240 and the LDCNT value for a 400 MHz clock speed is about 150. However, for an 800 MHz clock speed, the initial counter value might be 200, 220, 240, 260, or 280 depending upon the maximum operating speed of the integrated circuit as designated by the Device Speed value. The 280 initial counter value would be used for a slower integrated circuit to provide more time to issue the sequence of command signals which the 200 initial counter value would be used for a faster integrated circuit which was capable of issuing the sequence of command signals in a shorter time. After the initial counter value is loaded into the Counter 50, the Counter 50 decrements responsive to the CLK and CLK 90 signals from the clock circuit 28.

DEPR:
The NAND gates 66, 62 each receive as their third input the output of a NAND gate 70 which receives respective outputs from NAND gates 72, 74, and 76. The NAND gate 72 is enabled by the "400" signal from the register 30 whenever the clock speed is 400 MHz. Similarly, the NAND gate 74 is enabled whenever the clock speed is 600 MHz, and the NAND gate 76 is enabled whenever the clock speed is **800 MHz**. Additional circuitry may be used to accommodate other clock speed such as clock speeds of 100 MHz, 200 MHz, **300 MHz** and 700 MHz. The NAND gate 72 receives the F signal from the F.sub.4 stage of the shift register 34, the NAND gate 74 receives the F signal from the F.sub.5 output of the shift register 34, and the NAND gate 76 receives the F signal from the F.sub.6 stage of the shift register 34. Since only one of the NAND gates 72-76 will be enabled at any one time, only one of the NAND gates 72-76 will pass an F signal
generated by the shift register 34. In the example shown in FIG. 7, the "600" output of the register 30 is high thereby enabling the NAND gate 74. Thus, when the F.sub.5 signal is generated, the output of the NAND gate 74 goes low, as shown in the sixth line of FIG. 7. In response thereto, the output of the NAND gate 70 goes high for a similar period of time thereby causing the output of the NAND gate 66 to go low as shown in the next line of FIG. 7. Note that the output of the NAND gate 66 goes low for only one-quarter of a clock cycle since the NAND gate 66 is enabled for only that period, as shown in the third line of FIG. 7.

DEPR:
The remaining logic circuitry in FIG. 9 operates in substantially the same manner as the previously described circuitry. Specifically, the low order bits
from the Counter 50 are applied to a NOR gate 150 while the high order bits from the Counter 50 are applied to a NOR gate 152 either directly or, in the case of bit C.sub.4, through an inverter 154. The NOR gates 150, 152 each output a high whenever the Counter 50 outputs a counter value of "11110111" which is decimal 16. The outputs of the NOR gates 150, 152 are applied to a NAND gate 160 which is selectively enabled by the output of a NAND gate 162 coupled to the NAND gate 160 through an inverter 164. The NAND gate 160 is enabled whenever the EN input to the Decoders 56 is high and the register 30 (FIG. 3) outputs a high "400" signal indicative of a clock speed of 400 MHz. Thus, the column address enable command signal COL is generated at a counter value of 16 whenever the clock speed is 400 MHz. In a similar manner, other counter values are decoded to generate other command signals, with the correspondency between command signals and counter values being dependent on the **clock speed signal** SPEED.

DEPR:
The above-described operation of the SDRAM 180 is controlled by the Command Generator 26 responsive to high level command signals received on a control bus
160. These high level command signals, which are typically generated by a memory controller (not shown in FIG. 10), are a **clock enable signal** CKE*, a **clock signal** CLK, a chip select signal CS*, a write enable signal WE*, a row address strobe signal RAS*, and a column address strobe signal CAS*, which the "*" designating the signal as active low. However, other high level command signals may be used. In either case, the Command Generator 26 generates a sequence of command signals responsive to the high level command signals to carry out the function (e.g., a read or a write) designated by each of the high
level command signals. These command signals, and the manner in which they accomplish their respective functions, are conventional. Therefore, in the interest of brevity, a further explanation of these control signals will be omitted.

CLPR:
4. The command generator of claim 1, further comprising a counter load circuit
coupled to the counter and the clock speed indicator, the counter load circuit loading an initial count into the counter from which the counter increments or decrements responsive to the **clock signal**, the value of the initial count being
a function of the **clock speed signal**.

CLPR:
6. The command generator of claim 1 wherein the clock speed indicator comprises a register storing a plurality of clock speed values, one of the clock speed values being selectable to provide the **clock speed signal** corresponding thereto.

CLPR:
7. The command generator of claim 1, further comprising a counter enable circuit generating a counter enable signal to permit the counter to increment or decrement responsive to the **clock signal**, comprising:

CLPR:
12. The command generator of claim 10, further comprising a counter load

circuit coupled to the counter and the clock speed indicator, the counter load circuit loading an initial count into the counter from which the counter increments or decrements responsive to the **clock signal**, the value of the initial count being a function of the **clock speed signal**.

CLPR:
14. The command generator of claim 13, further comprising a clock speed indicator providing the **clock speed signal** corresponding to the speed of the **clock signal**.

CLPR:
15. The command generator of claim 14 wherein the clock speed indicator comprises a register storing a plurality of clock speed values, one of the clock speed values being selectable to provide the clock speed values being selectable to provide the **clock speed signal** corresponding thereto.

CLPR:
18. The command generator of claim 13, further comprising a counter load circuit loading an initial count into the counter from which the counter increments or decrements responsive to the **clock signal**, the value of the initial count being a function of the speed of the **clock signal**.

CLPR:
20. The command generator of claim 14, further comprising a counter enable circuit generating a counter enable signal to permit the counter to increment or decrement responsive to the **clock signal**, comprising:

CLPR:
23. The command generator of claim 22, further comprising a clock speed indicator providing the **clock speed signal** corresponding to the speed of the **clock signal**.

CLPR:
24. The command generator of claim 23 wherein the clock speed indicator comprises a register storing a plurality of clock speed values, one of the clock speed values being selectable to provide the **clock speed signal** corresponding thereto.

CLPR:
27. The command generator of claim 22, further comprising a counter load circuit loading an initial count into the counter from which the counter increments or decrements responsive to the **clock signal**, the value of the initial count being a function of the speed of the **clock signal**.

CLPR:
29. The command generator of claim 23, further comprising a counter enable circuit generating a counter enable signal to permit the counter to increment or decrement responsive to the **clock signal**, comprising:

CLPR:
34. The dynamic random access memory of claim 32, further comprising a counter
load circuit coupled to the counter and the clock speed indicator, the counter load circuit loading an initial count into the counter from which the counter increments or decrements responsive to the **clock signal**, the value of the initial count being a function of the **clock speed signal**.

CLPR:

36. The dynamic random access memory of claim 35, further comprising a clock speed indicator providing the **clock speed signal** corresponding to the speed of the **clock signal**.

CLPR:
37. The dynamic random access memory of claim 36 wherein the clock speed indicator comprises a register storing a plurality of clock speed values, one of the clock speed values being selectable to provide the **clock speed signal** corresponding thereto.

CLPR:
40. The dynamic random access memory of claim 35, further comprising a counter
load circuit loading an initial count into the counter from which the counter increments or decrements responsive to the **clock signal**, the value of the initial count being a function of the speed of the **clock signal**.

CLPR:
42. The dynamic random access memory of claim 35, further comprising a counter
enable circuit generating a counter enable signal to permit the counter to increment or decrement responsive to the **clock signal**, comprising:

CLPR:
46. The computer system of claim 45, further comprising a clock speed indicator providing the **clock speed signal** corresponding to the speed of the **clock signal**.

CLPR:
47. The computer system of claim 46 wherein the clock speed indicator comprises a register storing a plurality of clock speed values, one of the clock speed values being selectable to provide the **clock speed signal** corresponding thereto.

CLPR:
48. The computer system of claim 46, further comprising a counter enable circuit generating a counter enable signal to permit the counter to increment or decrement responsive to the **clock signal**, comprising:

CLPR:
52. The computer system of claim 45, further comprising a counter load circuit
loading an initial count into the counter from which the counter increments or decrements responsive to the **clock signal**, the value of the initial count being
a function of the speed of the **clock signal**.

CLPR:
57. The computer system of claim 55, further comprising a counter load circuit
coupled to the counter and the clock speed indicator, the counter load circuit loading an initial count into the counter from which the counter increments or decrements responsive to the **clock signal**, the value of the initial count being
a function of the **clock speed signal**.

CLPR:
58. A method of generating command signals for a memory device responsive to

a
clock signal, the method comprising generating a sequence of the command signals, the timing of the command signals corresponding to respective numbers of cycles of the **clock signal** that have occurred during the sequence, the number of clock cycles occurring between at least some of the command signals being determined by the **clock signal** frequency, the number of clock cycles occurring between command signals being higher for a higher **clock signal** frequencies and lower for lower **clock signal** frequencies.

CLPR:
59. The method of claim 58 wherein the timing of the command signals is adjusted so that the number of clock cycles occurring between at least some command signals is inversely proportional to the **clock signal** frequency whereby
time between the command signals is independent of the **clock signal** frequency.

CLPR:
60. A method of generating command signals for a memory device responsive to a
clock signal having at least one of a plurality of speeds, the method comprising:

CLPV:
a counter receiving a **clock signal** having at least one of a plurality of speeds, the counter generating a counter value that increments or decrements responsive to file **clock signal**;

CLPV:
a clock speed indicator providing a **clock speed signal** corresponding to the speed of the **clock signal**; and

CLPV:
a decoder coupled to the counter and the clock speed indicator, the decoder generating one of a plurality of sequences of command signals for the memory device, the command signals in each sequence corresponding to respective counter values, each of the sequences of command signals corresponding to a respective clock speed, the decoder selecting one of a plurality of the sequences responsive to the **clock speed signal**.

CLPV:
a counter start circuit comprising a clock detector detecting predetermined portions of the **clock signal**, and a variable delay enable circuit coupled to the clock detector and the clock speed indicator, the variable delay enable circuit selecting one of the detected predetermined portions of the **clock signal** subsequent to a flag signal after a predetermined number of cycles of the **clock signal**, the predetermined number of clock cycles corresponding to the
clock speed signal, the variable delay enable circuit generating the start signal responsive to the detected predetermined portion of the **clock signal** selected by the variable delay enable circuit.

CLPV:
a pulse generator coupled to the variable delay enable circuit, the pulse generator generating a pulse having a predetermined delay responsive to the detected predetermined portion of the **clock signal** selected by the variable delay enable circuit; and

CLPV:

a logic circuit coupled to the pulse generator, the logic circuit generating the start signal responsive to either the pulse generated by the pulse generator or the detected predetermined portion of the **clock signal** selected by
the variable delay enable circuit.

CLPV:
a clock speed indicator providing a **clock speed signal** corresponding to the speed of a **clock signal** having at least one of a plurality of clock speeds; and

CLPV:
a sequencer coupled to the clock speed indicator and generating a sequence of command signals for the memory device responsive to the **clock signal,** the timing of the command signals in the sequence being determined by the **clock speed signal** whereby the timing and nature of the command signals correspond to
the clock speed.

CLPV:
a counter receiving the **clock signal** and generating a counter value that increments or decrements responsive to the **clock signal**; and

CLPV:
a decoder coupled to the counter and the clock speed indicator, the decoder generating one of a plurality of sequences of command signals for the memory device, the command signals in each sequence corresponding to respective counter values, each of the sequences of command signals corresponding to a respective clock speed, the decoder selecting one of a plurality of the sequences responsive to the **clock speed signal**.

CLPV:
a counter receiving a **clock signal** having at least one of a plurality of speeds, the counter generating a counter value that increments or decrements responsive to the **clock signal**; and

CLPV:
a decoder coupled to the counter, the decoder generating one of a plurality of sequences of command signals for the memory device with each of the command signals in each sequence being generated at a time corresponding to a respective counter value, the decoder selecting one of a plurality of the sequences responsive to a **clock speed signal** indicative of the clock speed.

CLPV:
a counter start circuit comprising a clock detector detecting predetermined portions of the **clock signal,** and a variable delay enable circuit coupled to the clock detector and the clock speed indicator, the variable delay enable circuit selecting one of the detected predetermined portions of the **clock signal** subsequent to a flag signal after a predetermined number of cycles of the **clock signal,** the predetermined number of clock cycles corresponding to the
clock speed signal, the variable delay enable circuit generating the start signal responsive to the detected predetermined portion of the **clock signal** selected by the variable delay enable circuit.

CLPV:
a pulse generator coupled to the variable delay enable circuit, the pulse generator generating a pulse having a predetermined delay responsive to the

detected predetermined portion of the **clock signal** selected by the variable delay enable circuit; and

CLPV:
a logic circuit coupled to the pulse generator, the logic circuit generating the start signal responsive to either the pulse generated by the pulse generator or the detected predetermined portion of the **clock signal** selected by
the variable delay enable circuit.

CLPV:
a counter receiving a **clock signal** having at least one of a plurality of clock speeds, the counter generating a counter value that increments or decrements responsive to the **clock signal**; and

CLPV:
a counter start circuit comprising a clock detector detecting predetermined portions of the **clock signal**, and a variable delay enable circuit coupled to the clock detector and the clock speed indicator, the variable delay enable circuit selecting one of the detected predetermined portions of the **clock signal** subsequent to a flag signal after a predetermined number of cycles of the **clock signal**, the predetermined number of clock cycles corresponding to the
clock speed signal, the variable delay enable circuit generating the start signal responsive to the detected predetermined portion of the **clock signal** selected by the variable delay enable circuit.

CLPV:
a pulse generator coupled to the variable delay enable circuit, the pulse generator generating a pulse having a predetermined delay responsive to the detected predetermined portion of the **clock signal** selected by the variable delay enable circuit; and

CLPV:
a logic circuit coupled to the pulse generator, the logic circuit generating the start signal responsive to either the pulse generated by the pulse generator or the detected predetermined portion of the **clock signal** selected by
the variable delay enable circuit.

CLPV:
a clock circuit generating a **clock signal** that may have one of a plurality of speeds;

CLPV:
a clock speed indicator providing a **clock speed signal** corresponding to the speed of the **clock signal**;

CLPV:
a command signal generator coupled to the clock speed indicator and generating a sequence of command signals responsive to the **clock signal**, including the first, second and third set of command signals, the timing of the command signals in the sequence being determined by the **clock speed signal**.

CLPV:
a counter receiving the **clock signal** and generating a counter value that increments or decrements responsive to the **clock signal**; and

CLPV:
a decoder coupled to the counter and the clock speed indicator, the decoder generating one of a plurality of sequences of command signals for the memory device, the command signals in each sequence corresponding to respective counter values, each of the sequences of command signals corresponding to a respective clock speed, the decoder selecting one of a plurality of the sequences responsive to the **clock speed signal**.

CLPV:
a clock circuit generating a **clock signal** having at least one of a plurality of
speeds;

CLPV:
a counter receiving a **clock signal,** the counter generating a counter value that
increments or decrements responsive to the **clock signal**; and

CLPV:
a command generator coupled to the counter, the command generator generating the first, second, and third sets of command signals, each command signal corresponding to a respective counter value, the command generator generating one of a plurality of sequences of command signals, including the first, second, and third set of command signals, each of the sequences of command signals corresponding to a respective clock speed, the command generator selecting one of a plurality of the sequences responsive to a **clock speed signal** indicative of the clock speed.

CLPV:
a counter start circuit comprising a clock detector detecting predetermined portions of the **clock signal,** and a variable delay enable circuit coupled to the clock detector and the clock speed indicator, the variable delay enable circuit selecting one of the detected predetermined portions of the **clock signal** subsequent to a flag signal after a predetermined number of cycles of the **clock signal,** the predetermined number of clock cycles corresponding to the
clock speed signal, the variable delay enable circuit generating the start signal responsive to the detected predetermined portion of the **clock signal** selected by the variable delay enable circuit.

CLPV:
a pulse generator coupled to the variable delay enable circuit, the pulse generator generating a pulse having a predetermined delay responsive to the detected predetermined portion of the **clock signal** selected by the variable delay enable circuit; and

CLPV:
a logic circuit coupled to the pulse generator, the logic circuit generating the start signal responsive to either the pulse generated by the pulse generator or the detected predetermined portion of the **clock signal** selected by
the variable delay enable circuit.

CLPV:
a counter start circuit comprising a clock detector detecting predetermined portions of the **clock signal,** and a variable delay enable circuit coupled to the clock detector and the clock speed indicator, the variable delay enable circuit selecting one of the detected predetermined portions of the **clock**

signal subsequent to a flag signal after a predetermined number of cycles of the **clock signal**, the predetermined number of clock cycles corresponding to the **clock speed signal**, the variable delay enable circuit generating the start signal responsive to the detected predetermined portion of the **clock signal** selected by the variable delay enable circuit.

CLPV:
a pulse generator coupled to the variable delay enable circuit, the pulse generator generating a pulse having a predetermined delay responsive to the detected predetermined portion of the **clock signal** selected by the variable delay enable circuit; and

CLPV:
a logic circuit coupled to the pulse generator, the logic circuit generating the start signal responsive to either the pulse generated by the pulse generator or the detected predetermined portion of the **clock signal** selected by the variable delay enable circuit.

CLPV:
a counter receiving the **clock signal** and generating a counter value that increments or decrements responsive to the **clock signal**; and

CLPV:
a decoder coupled to the counter and the clock speed indicator, the decoder generating one of a plurality of sequences of command signals for the memory device, the command signals in each sequence corresponding to respective counter values, each of the sequences of command signals corresponding to a respective clock speed, the decoder selecting one of a plurality of the sequences responsive to the **clock speed signal**.

CLPV:
selecting one of the command signal sequences as a function of the speed of the **clock signal**; and

CLPW:
a clock circuit generating a **clock signal** having at least one of a plurality of speeds;

CLPW:
a counter receiving a **clock signal**, the counter generating a counter value that increments or decrements responsive to the **clock signal**; and

CLPW:
a command generator coupled to the counter, the command generator generating the first, second, and third set of command signals, each of the command signals being generated at a time corresponding to a respective counter value, the command generator generating one of a plurality of sequences of command signals, including the first, second, and third set of command signals, each of the sequences of command signals corresponding to a respective clock speed, the command generator selecting one of a plurality of the sequences responsive to a

clock speed signal indicative of the clock speed.

CLPW:
a clock circuit generating a **clock signal** that may have one of a plurality of speeds;

CLPW:
a clock speed indicator providing a **clock speed signal** corresponding to the speed of the **clock signal**;

CLPW:
a command signal generator coupled to the clock speed indicator and generating a sequence of command signals responsive to the **clock signal**, including the first, second and third set of command signals, the timing of the command signals in the sequence being determined by the **clock speed signal**.